the gates of devices M10 130 and M20 140. This differential input voltage creates a differential current in the drains of the input devices, which appears across the inductive loads, resulting in an output voltage Vout between lines 165 and 170. The terms line and node are used interchangeably throughout this document.

Cmt A1

The performance of this RF buffer is limited. Specifically, this circuit has an undesirably high supply current. For example, when the input voltage is at a maximum such that the voltage on line 135 is much higher in the voltage on line 145, devices M10 130 conducts the current of the current source 150, steering it through load L1 110. This current does not pass through the second load device L2 120, thus the supply current is seen by only one half the differential load L1 110 and L2 120.

When the voltage Vin is near zero, the voltage on line 135 is equal to, or nearly equal to, the voltage on line 145, and the currents in devices M10 130 and M20 140 are approximately balanced. At this time, there is no differential current in the drains of the input devices, and the rate of change of current in the loads L1 110 and L2 120 is minimal. Thus, the bias current from current source 150 is wasted, since at this point it does not contribute to the output swing. Furthermore, this circuit has limited output voltage range. Since the loads are inductive, the output lines 165 and 170 swing above and below the supply voltage VDD provided on line 160. But there is a limit to how low an output node can swing. Specifically, if the voltage at line 170 decreases, device M10 130 enters its triode region, reducing the head room from current source 150, either reducing its output or shutting it off. Accordingly, Vin should be biased to provide sufficient head room for the operation of current source 150, and the output swing should be limited to avoid driving input devices M10 130 and M20 140 into their triode regions.

Please replace the paragraph starting on page 4 line 31 and ending on page 5 line 4 with the following paragraph:

A2

The drain currents of devices M10 130 and M20 140 are shown as waveforms 220 and 230 respectively. Each current is plotted against a Y axis, 222 and 232, corresponding to current amplitude, and an X axis, 224 and 234, corresponding to

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cmt A2

time. If the input voltage is of sufficient magnitude, then each current waveform has a maximum value of the current in current source 150, ICS, and a minimum value of zero. These two current waveforms are 180 degrees out of phase with each other. The current waveform in M10 130 is out of phase with the input voltage Vin, while the drain current of M20 140 is in phase.

Please replace the two paragraphs starting on page 5 line 20 and ending on page 6 line 5 with the following two paragraphs:

A3

Figure 3 is a simplified schematic for an RF buffer amplifier 300 consistent with an embodiment of the present invention. Included are switches S1 310, S2 320, S3 330, and S4 340, inductive load L1 350, and capacitor C10 355. Inductor L 1 350 and capacitor C10 355 form a tank circuit. The capacitor C10 355 may be a real capacitor, it may be the capacitance of the switches plus the capacitance of the interconnect between the inductor and switches, or it may be a combination of the two. A first supply voltage VDD is applied on line 360. A second supply voltage VSS is applied on line 370. In one embodiment of the present invention VDD is equal to 1.8 V and VSS is ground or 0 Volts. Alternately, VDD may be other supply voltages. For example, VDD may be equal to 2.5 or 3.3 Volts. An output voltage is generated across the inductive load L1 350, appearing at lines 380 and 390.

An input signal controls the state of the four switches. When the input has a first polarity, switches S4 340 and S1 310 are closed, and S2 320 and S3 330 are open. Current flows from VDD applied on line 360, through S1 310, through the tank circuit L1 350 and C10 355, into S4 340, returning to ground or VSS on line 370. When the input has a second polarity, S2 320 and S3 330 are closed while S1 310 and S4 340 are open. In this state current flows from the supply voltage VDD on line 360, through the switch S2 320, through the tank circuit L1 350 and C10 355, into switch S3 330, returning to ground or VSS on line 370. The change in current through the tank circuit L1 350 and C10 355 creates a voltage output between the lines 380 and 390.

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Please replace the paragraph starting on page 9 line 3 and ending on page 9 line 11 with the following paragraph:

Figure 5 is a schematic showing the circuit components in the current path discussed above. Again, as the input voltage increases, the voltage on line 415 increases, and the gate voltage of device M2 420 increases. Device M2 420 conducts an increasing amount of current which flows through cascode device M4 440. This current flows through inductor L1 480. Accordingly, the voltage at line 445 decreases, while the voltage at line 455 increases. This decreasing voltage at line 445 turns on device M7 470, which conducts current back through inductor L1 480. Again, as the voltage on line 445 continues to decrease, the device M7 4 70 turns on harder, thus increasing the voltage at 455 and decreasing voltage at 445 at an increasing rate.

Please replace the paragraph starting on page 9 line 19 and ending on page 9 line 25 with the following paragraph:

Figure 6 illustrates the current and voltage waveforms at some of the nodes in the circuit of Figure 4. Input voltage waveform 610 is plotted as a function of time along X axis 614. Input waveform 610 is an example of a signal Vin which may be applied between lines 415 and 425. Input waveform 610 has an average value of zero, a peak voltage of Vinmax, and a minimum voltage of Vinmin. Input waveform 610 is shown as being approximately sinusoidal, as if generated by a voltage controlled oscillator (VCO) or similar circuit.

Please replace the paragraph starting on page 9 line 26 and ending on page 9 line 31 with the following paragraph:

When Vin is high, that is, Vin is between the values of Vinmax and approximately zero, a current is generated in the drain of device M2. When Vin is negative, that is, Vin has a value between approximately zero and Vinmin, the drain current of device M2 is approximately zero. As waveform 610 increases, the drain current in M2 increases geometrically and reaches a maximum value shown here as I1.